CLAIMS

I claim:

1. A semiconductor device comprising:
a common substrate;
an SRAM device implemented on the common substrate and isolated by a first isolation technique; and
a flash EPROM device implemented on the common substrate and isolated by a second isolation technique.

2. The semiconductor device according to claim 1 wherein the first isolation technique is an STI technique.

3. The semiconductor device according to claim 1 wherein the second isolation technique is a LOCOS isolation technique.

4. The semiconductor device according to claim 1 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

5. A system for allowing different types of isolation techniques during fabrication of a semiconductor device, comprising:
a common substrate having a first portion on which a first isolation technique is implemented during processing and a second portion on which a second isolation technique is implemented during processing;

an SRAM device implemented on the first portion of the substrate; and
a flash EPROM device implemented on the second portion of the substrate.

6. The system according to claim 5 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

7. The system according to claim 5 wherein the first isolation technique is an STI technique.

8. The system according to claim 5 wherein the second isolation technique is a LOCOS technique.

9. A semiconductor device comprising:
a common substrate having a first portion on which an STI isolation technique is implemented during processing and a second portion on which a LOCOS isolation technique is implemented during processing;
an SRAM device implemented on the first portion of the substrate; and
a flash EPROM device implemented on the second portion of the substrate.

10. The semiconductor device according to claim 9 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

11. A method of integrating two types of isolation techniques on a single substrate during fabrication of a semiconductor device, comprising the steps of:

implementing a LOCOS isolation technique in a LOCOS area on the substrate;

implementing a first semiconductor device in the LOCOS area on the substrate;

implementing an STI technique in an STI area on the substrate; and

implementing a second semiconductor device in the STI area on the substrate.

12. The method according to claim 11 further comprising the step of masking the LOCOS area when the step of implementing the STI technique is performed.

13. The method according to claim 11 further comprising the step of masking the STI area when the step of implementing the LOCOS technique is performed.

14. The method according to claim 11 wherein the first semiconductor device is a flash EPROM device, and the second semiconductor device is an SRAM device.

15. A method of fabricating a semiconductor device including both an SRAM device and a flash EPROM device, comprising the steps of:

implementing a LOCOS isolation technique in a LOCOS area on the substrate;

implementing the flash EPROM device in the LOCOS area on the substrate;

implementing an STI technique in an STI area on the substrate; and

implementing the SRAM device in the STI area on the substrate.

16. The method according to claim 15 further comprising the step of masking the LOCOS area when the step of implementing the STI technique is performed.

17. The method according to claim 15 further comprising the step of masking the STI area when the step of implementing the LOCOS technique is performed.